High Efficiency RF Energy Harvester for IoT Embedded Sensor Nodes

Stylianos D. Assimonis*, Spyridon N. Daskalakis†‡, Vincent Fusco*, Manos M. Tentzeris† and Apostolos Georgiadis‡
*School of Electronics, Electrical Engineering & Computer Science, Queen's University, Belfast, BT39DT, UK
Email: s.assimonis@qub.ac.uk, v.fusco@ecit.qub.ac.uk
†School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332–0250
Email: daskalakispiros@gatech.edu, etentze@ece.gatech.edu
‡School of Engineering & Physical Sciences, Heriot-Watt University, Edinburgh, EH144AS, UK
Email: apostolos.georgiadis@ieee.org

***Abstract*—This work presents a high efficiency, co-planar and low-complexity RF-to-dc rectifier of one diode, which is able to be directly connected, i.e., without a matching network, to a co-planar antenna, e.g., to a dipole or loop antenna. The rectifier was designed to optimally operate at 868 MHz and for low power input. Specifically, it presents 54.82% RF-to-dc efficiency for -20 dBm power input, while for -14.4 dBm the system is able to supply continuously, i.e., with any boost converter, a backscatter sensor node with power consumption of 20 μW.**

I. Introduction

Over the last years, RF energy harvesting, i.e., the use of ambient RF power in order to supply electrical devices [1], is gaining ground, because of the rapid growing of new wireless mobile technologies, e.g., Wireless Sensor Networks (WSN), Radio Frequency Identification (RFID) and Multi-Input Multi-Output (MIMO) systems. In a conventional RF harvester, an antenna captures the unused RF energy and the latter is transformed to dc through a rectification system, which consists of one or more diodes. Based on the literature [2]–[7], for low power input, the RF-to-dc efficiency, i.e., the fraction of the RF power input which finally is transformed to dc power, rarely exceed 30%. In order to increase the efficiency, the losses on the rectifier should be minimized.

The contribution of this work is that proposes a new co-planar design for the rectifier, which uses only one diode (the number of the diodes increases the losses, and thus, decreases the efficiency [6], [7]) and is able to be directly connected to an impedance matched antenna, without using any extra matching network, leading to further reduction of the losses. The proposed harvester, because of its high efficiency and low-complexity, is a perfect candidate for the supply of small electrical devises, such as battery-less backscatter sensor nodes [8].

II. Rectifier

The rectifier's topology and schematic is presented in Fig. 1: it is co-planar (i.e., absence of ground plane) in order to facilitate easy connection with a co-planar antenna and consists of a single diode in series configuration with the load R (capacitor C is used for voltage stability), and thus, it performs half-wave RF-to-dc rectification. The "HSMS285b" diode (Avago Technologies, Inc.) was chosen in our simulations, which took place through the commercial ADS software (Keysight Technologies), while for substrate the Taconic TLY-5 ($\epsilon_r = 2.17$, $\tan\delta = 0.0009$) with thickness of 0.508 mm was used. The rectifier's RF-to-dc efficiency is defined as

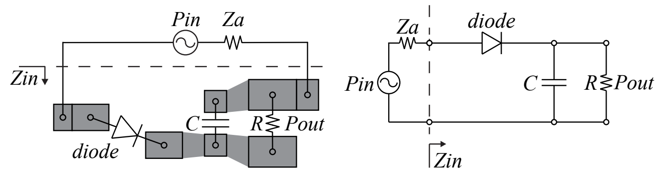
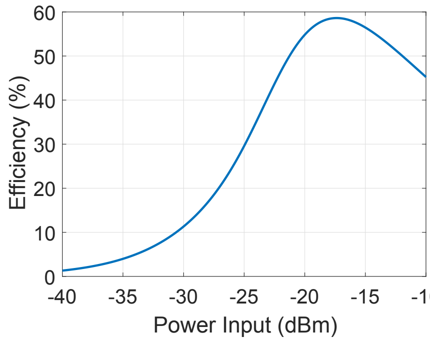


Fig. 1. The rectifier's topology (a) and circuit schematic (b): it consists of a diode in series configuration with a load, performing half-wave rectification. In this work the "HSMS285b" diode was used.

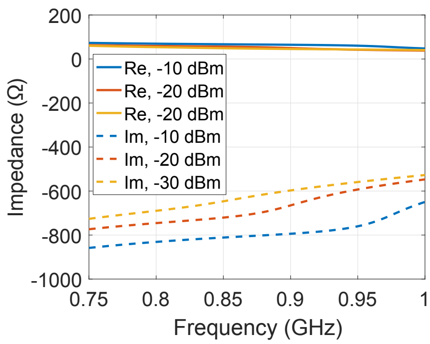
$$\eta = \frac{P_{\mathrm{dc}}}{P_{\mathrm{RF}}} \tag{1}$$

where, P_{dc} is the dc power output and P_{RF} is the RF power input. Efficiency is a function not only of the operating frequency, but also of the power input and the load, since the structure is non-linear because of the presence of the diode. In this work, the rectifier was designed to optimally operate for low power input of -20 dBm at 868 MHz, taking into account the allocated UHF RFID frequencies in Europe. Thus, during the design procedure, optimization was performed with fitness function the η and degrees of freedom the RF source impedance Z_a and the load R, while frequency and power input was fixed at 868 MHz and -20 dBm, respectively, while $C = 100$ pF. Finally, the efficiency was maximized for $Z_a = 54.6 + j707.6$ Ω and $R = 15.4$ kΩ.

Fig. 2a depicts the efficiency versus power input: for -20 dBm $\eta = 54.82\%$, while the maximum of 58.6% occurs for power input of only -17.4 dBm. The rectifier's input impedance versus frequency for various levels of power input is depicted in Fig. 2b. It is evident that the rectifier is non-linear and for -20 dBm $Z_{in} = 54.6 - j707.6$ Ω, and thus the source is conjugate matched with the rectifier, as expected,

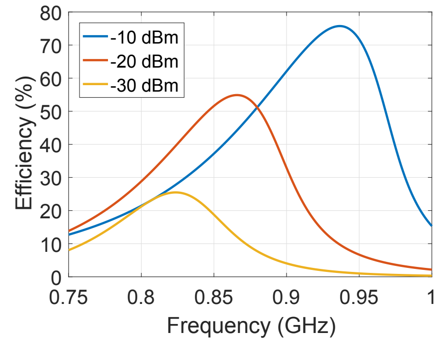


(a)

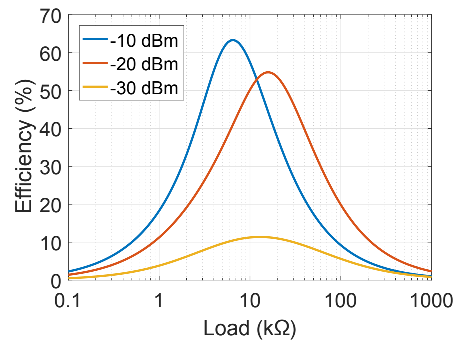


(b)

Fig. 2. Simulated rectifier's RF-to-dc efficiency versus power input at 868 MHz (a) and the real (Re) and the imaginary (Im) part of the rectifier's input impedance versus frequency for various levels of power input (b). The load R at both cases is 15.4 kΩ and for the source is $Z_a = 54.6 + j707.6$ Ω.



(a)



(b)

Fig. 3. Simulated rectifier's efficiency versus frequency (a) and load (b) for various levels of power input: when the frequency varies the load is fixed at 15.4 kΩ, while when the latter varies, the frequency is fixed at 868 MHz. At both cases, $Z_a = 54.6 + j707.6$ Ω.

based on the optimization procedure. Fig. 3a and 3b depicts again the RF-to-dc efficiency, but now versus frequency and load, respectively, for various levels of input power: when the frequency varies the load is fixed at 15.4 kΩ, while when the load varies the frequency is fixed at 868 MHz. In general, for higher levels of power input the maximum efficiency takes place in higher frequency and lower output load. It is noted that in all cases the source is impedance matched with the rectifier, i.e., $Z_a = 54.6 + j707.6$ Ω.

III. Application

For -14.4 dBm power input the RF-to-dc efficiency is 55.41% (Fig. 2a), and thus, the rectifier serves more than 20 μW to the load. On the other hand, in [8] authors presented a backscatter sensor node with power consumption of the order of 20 μW. Thus, the proposed rectifier is able to supply continuously, i.e., without the use of any boost converter, battery-less backscatter sensor nodes.

IV. Conclusion

In this work first presented a new, co-planar, low-complexity and very high efficiency rectifier. The latter, which is able to be directly connected to a co-planar antenna, is perfect candidate for the supply of battery-less backscatter sensor nodes, and thus for IoT applications, in general.

V. Acknowledgment

This work was supported by the UK Engineering and Physical Sciences Research Council (EPSRC) EP/S007954/1.

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